SEU Evaluation of SRAM Memories for Space Applications.

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Abstract

SEU cross-sections were obtained for three different SRAM memories. The 1 Mbit White Electronics WMS128k8, the 256 kbit Austin MT5C2564 and the 256 kbit Austin MT5C2568 SRAMs were tested. The SEU thresholds, respectively were 1 MeV cm^2/mg, 1.4 MeV cm^2/mg, and 1.8 MeV cm^2/mg. SEL thresholds were also obtained. These were 37 MeV cm^2/mg, 37 MeV cm^2/mg and 59 MeV cm^2/mg, respectively.

I. Introduction

Due to the ever increasing need for viable space avionics systems, more and more Commercial-Off-the-Shelf (COTS) parts are being investigated for application in radiation environments. Advanced, high density SRAMs are candidates especially since the memory density and speed requirements for upcoming the missions to Mars and outer planet probes are very demanding. SRAM technology continues to present an attractive operable device for use in remote systems [1]. This is the driving force behind this study.

II. SRAM Devices

CMOS-based SRAM technology has been investigated for SEE effects for some time [2]. Studies have concentrated on areas as far ranging as models to real-time flight studies [3,4]. Since SRAM technology continues to be attractive for avionics systems, the SEE response is of great importance [2-4]. The primary consideration of many of the studies is the characterization of the SEU and SEL cross section curves and the thresholds for the respective phenomenon [5]. Latch-ups present the added concern of catastrophic damage, which is very important.

In this study similar investigations are conducted [6]. The three different SRAM devices were used in this study. The White Electronics WMS128k8, the Austin MT5C2564 and the Austin MT5C2568 SRAMs were tested. Table 1 shows basic features of the devices. Three of each device type were tested for response under heavy ions. The devices were encased in lidded DIP packages, which were easily delidded for exposure to heavy ions.

Table 1. Properties of the SRAM devices under test.

Device	Man.	Size	Code	Tech.	SNs
WMS128K8	White	128kx8	WMS128 K8-55CI	CMOS	S0964 S0965 S0966
MT5C2564	Austin	64kx4	MT5C256 4C-35/CT	CMOS	S0954 S0955 S0956
MT5C2568	Austin	32kx8	MT5C256 8C-25/CT	CMOS	S0959 S0960 S0962

III. Test Setup And Procedure

The test equipment was comprised of two PCs, a power supply, and a specially designed test board. One PC controlled a HP6629A power supply. This allowed precision voltage control and latch-up detection and protection since the PC had millisecond control over the operation of the power supply. Latch-ups were recorded in a separate file during the test.

A dedicated PC controlled the test circuit board designed specifically for this SRAM test to read and write to the DUTs. Custom daughter boards allow each SRAM type to be tested by the same test board. The address of each DUT could be accessed randomly and the address space can be accessed at a rate of 2185 addresses per second. This setup allows complete freedom to interact with the DUT. The address of a failure and the value at that address were recorded in a file for each run. This allowed for any structure in the SEEs or predilection for certain pattern failure or type of SEU to be observed. A depiction of the setup used is shown in Figure 1. Testing was done at the Brookhaven National Laboratory and Texas A&M cyclotrons.

Table 2. Ions used in testing.

Species	Site	LET	Angles used
Argon	TAM	5.4	0, 45, 50, 55, 60
Argon	TAM	10.0	0, 30, 45
Argon	TAM	15.0	0, 30, 45
Chlorine	BNL	11.4	0, 45, 55, 60
Nickel	BNL	26.6	0, 45, 55, 60
Iodine	BNL	59.9	0, 45, 55, 60
Carbon	BNL	1.4	0, 45, 55, 60

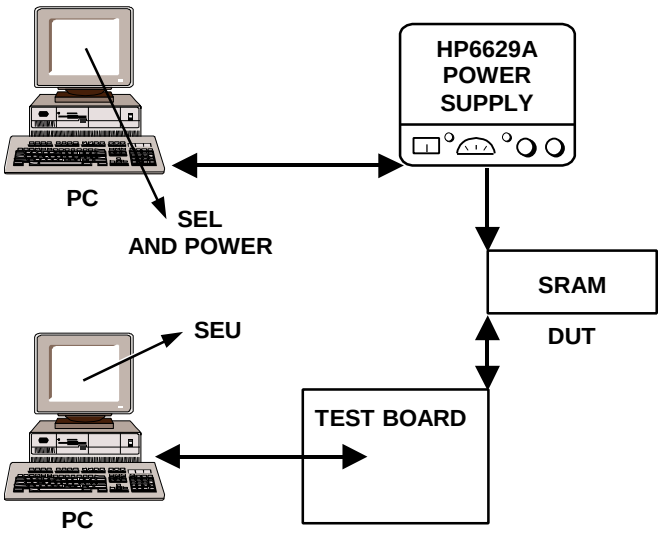

Figure 1. A block diagram of the test system.

For this test, most of the radiation runs are done when the DUT was in stand by mode with a known pattern written in the DUT. The PC cycled through the address space of the DUT, stored address, which exhibited an error, along with the error value, and rewrote the correct pattern to the address. The most common pattern written to the device was a checkerboard pattern, i.e. an 8-bit address would have 170 in address 0, 85 in address 1, 170 in address 2, and so on. Some tests were done while actively reading or writing data to test for susceptibility to SEE during such processes.

The Vdd voltage was always set to 5 volts and the operating temperature was approximately 25 °C throughout the study.

IV. Heavy Ion Results

A. SEU Results

All of the devices had similar results. All of the devices were programmed and read using the same handshaking protocol. To measure any catastrophic effects, one of each of the devices was exposed to more than 10^5 iodine ions (LET 60 MeV cm^2/mg) with no latch-up protection. All of these DUTs were seen to work after the exposure. No stuck bits or residual programming problems were seen in any of the devices. Error bars on all graphs are based on Poisson counting statistics.

Some exposures were done during programming or reading to determine any contribution these processes. No dependence was seen. Some devices show a zero to one SEU than the one to zero SEU. In general, devices exhibited a larger probability of one to zero upsets.

White Electronics WMS128K8

The cross-section curve is shown in Figure 2. The cross-section increases steadily with LET, which is typical of many SRAMs. A Weibull based threshold curve is fit to the data. This device was the softest of the three tested in this study. This device showed a 1.8 % predilection toward one to zero upsets.

Austin MT5C2568

The cross section of the device also responded in a smooth regular way, which is shown in Figure 3. The device actually did not upset at 2.88 MeV cm^2/mg, but the fluence was too low to assume SEU immunity. The actual cross section would be below the plotted value and this is the significance of the error bar. The part showed no anomalous readings. This device demonstrated a 1.2% bias to one to zero SEUs. A Weibull based threshold curve is fit to the data.

Austin MT5C2564

The cross-section curve is shown in Figure 4. The cross-section reached saturation quickly. This device was the softest of the three tested in this study. This device showed no predilection toward one to zero upsets. A Weibull based threshold curve is fit to the data.

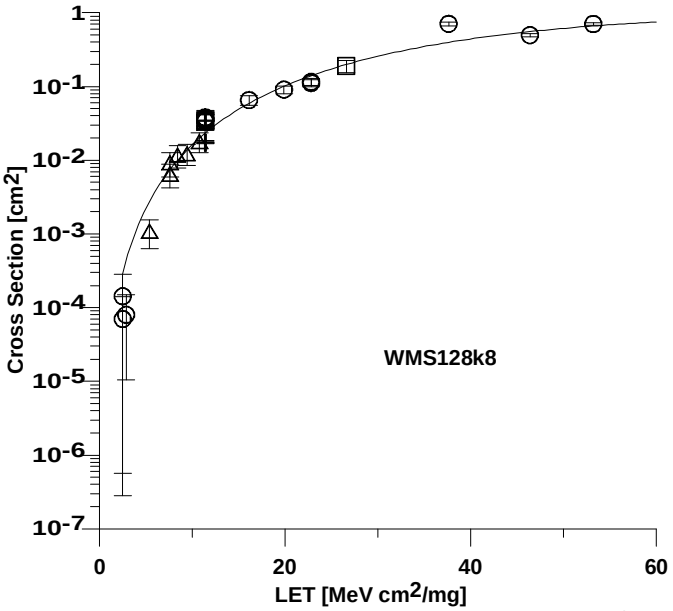

Figure 2. The SEU vs. LET cross section curve for a typical WMS128K8 SRAM. Triangles are points taken at TAM. Circles and squares were taken at BNL. The error bars are estimated from Poisson counting statistics.

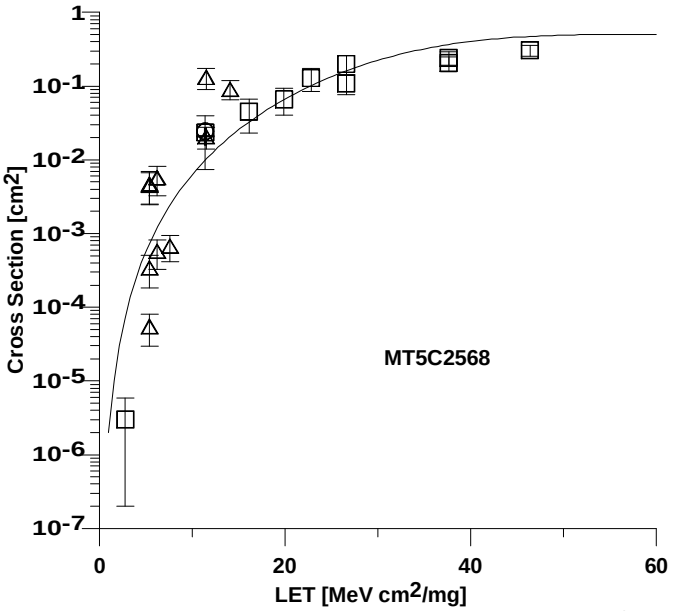

Figure 3. The SEU vs. LET cross section curve for a typical MT5C2568 SRAM. Triangles are points taken at TAM. Circles and squares were taken at BNL. The error bars are estimated from Poisson counting statistics.

B. SEU Thresholds

The LET threshold of the device was found using two definitions. The typical 10% of saturation value definition was used. Another definition was the LET at which the cross-section would be the inverse of the number of bits multiplied by the estimated die area. This is approximately 10^{-7} cm^2 for all devices. The WMS128K8 devices extrapolate the threshold SEU to 1 MeV cm^2/mg. The threshold for MT5C2568 extrapolates to 1.8 MeV cm^2/mg. The MT5C2564

SEU threshold is 1.41 MeV cm^2/mg. Both LET thresholds are shown in Table 3 along with the SEL thresholds.

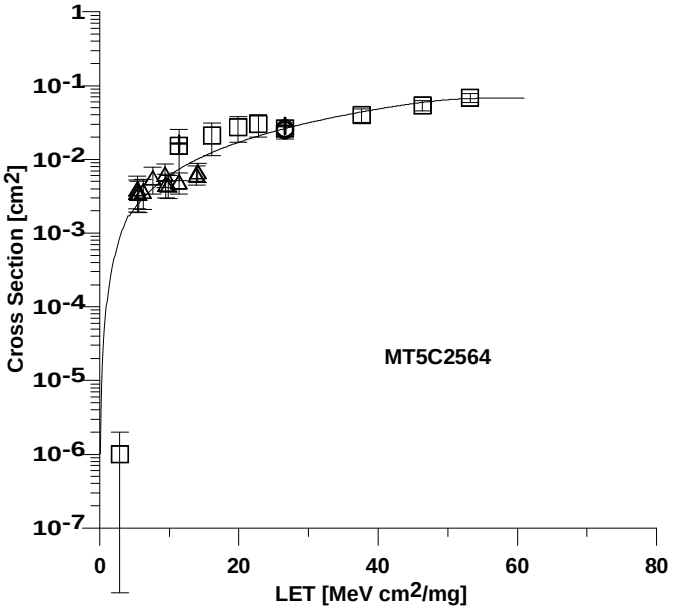

Figure 4. The SEU vs. LET cross section curve for a typical MT5C2564 SRAM. Triangles are points taken at TAM. Circles and squares were taken at BNL. The error bars are estimated from Poisson counting statistics. The fit is a modified Weibull.

C. SEL Results

The devices proved relatively immune to SEL effects. Figure 5 shows the cross-section curve of the SELs. Latch-up levels were generally set at the limits in the specifications. Latch-ups increase with LET but the statistics were generally too low to generate meaningful fits.

V. Conclusion

The radiation testing of these SRAMs has shown that CMOS SRAM technology is very sensitive to SEU and less sensitive to SEL. The devices are mostly excluded from use in a severe radiation environment.

Acknowledgments

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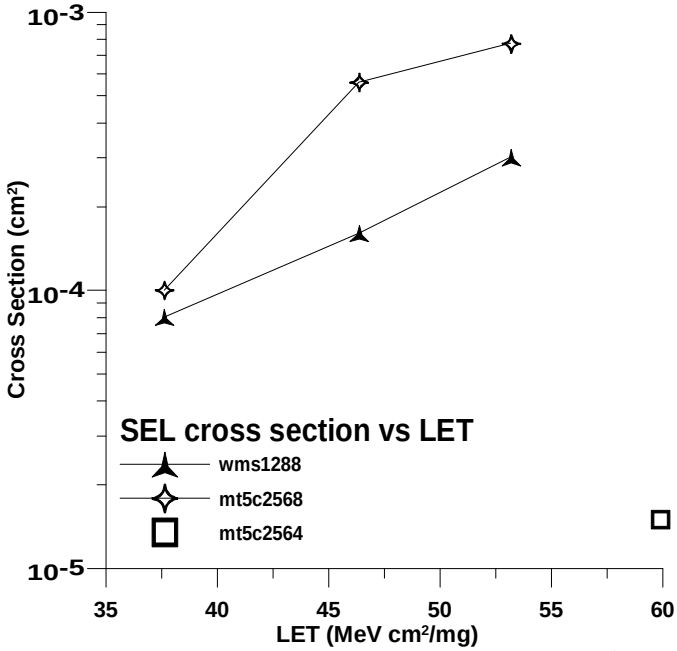

Figure 5. The SEL vs. LET cross section curve for the SRAMs studied. Note expanded scale.

Table 2. Thresholds for various SRAMs.

Device	SEU Threshold Using 10% of Sat. (MeV cm^2/mg)	SEU Threshold 10^{-7} cm^{-2} floor. (MeV cm)	SEL Threshold (MeV cm^2/mg)
WMS128k8	1.01	17	37.61806
MT5C2568	1.88	15	37.61806
MT5C2564	1.40	10	58

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